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(71) Applicant: **GEC-MARCONI LIMITED**
The Grove,
Warren Lane
Stanmore, Middlesex HA7 4LY (GB)

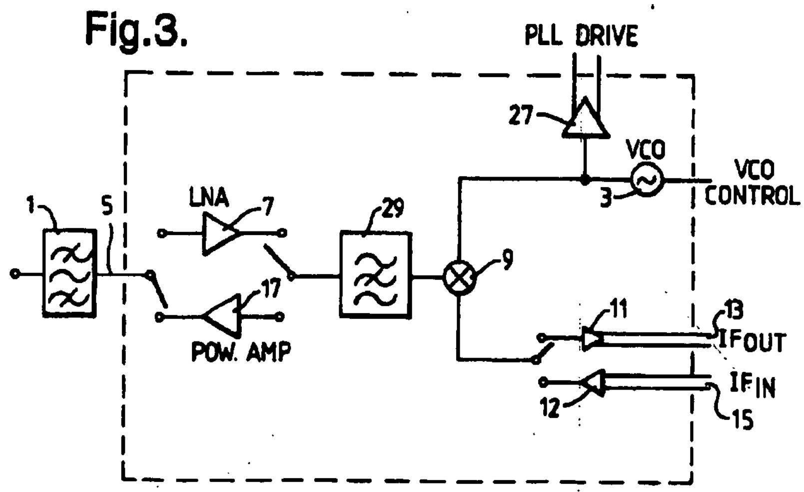
(72) Inventor: **Devlin, Liam Michael**
58 Beech Avenue
Abington, Northampton, NN3 2JG (GB)
Inventor: **Buck, Brian Jeffrey**
2 New Street
Weedon, Northampton NN7 4QS (GB)

(74) Representative: **Pope, Michael Bertram Wingate**
The General Electric Company, p.l.c.
GEC Patent Department
Waterhouse Lane
Chelmsford, Essex CM1 2QX (GB)

(54) An integrated transceiver circuit packaged component.

(57) An integrated transceiver circuit packaged component including a transceiver circuit having a band-stop filter (29) provided therein for filtering both the received and transmitted signals to remove unwanted components therefrom.

Fig.3.



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This invention relates to an integrated transceiver circuit packaged component.

One known such component is shown in Figure 1 of the accompanying drawings together with an external filter 1. The transceiver has two modes of operation, transmit and receive. In both modes a local oscillator signal is generated by an on-chip voltage controlled oscillator (VCO) 3.

In the receive mode signals enter the transmit/receive (T/R) common port 5 at the RF frequency. The signal level is boosted by the low noise amplifier (LNA) 7 with the addition of very little noise. The off-chip band pass filter 1 then rejects all of the noise power at the image frequency (local oscillator frequency (LO) - intermediate frequency (IF), for an RF signal at LO + IF). Without filter 1 the image noise power would be down-converted to the IF along with the signal (and noise) at the RF frequency. A mixer 9 multiplies the RF and VCO signals and generates an IF signal at a frequency RF - LO (assuming RF is greater than LO). The IF signal is then amplified by a differential amplifier 11 prior to its output at port 13.

In the transmit mode a differential input signal at the IF frequency is input at port 15 and amplified by differential amplifier 12. Mixer 9 multiplies the output of amplifier 12 with the VCO signal to generate two 'sidebands' at LO - IF and LO + IF. Assuming the RF signal is at LO + IF, then this is the wanted sideband and the LO - IF signal is termed the unwanted sideband. Filter 1 is used to reject the unwanted sideband and any other spurious mixing products/harmonics. The wanted RF signal is then routed back on chip and through a power amplifier 17 prior to output at the T/R common port 5.

The transceiver circuit further comprises an amplifier 23 connected to the output of VCO 3 for provding a phase locked loop (PLL) drive at output port 25 of the package.

With reference to Figure 2 of the accompanying drawings, microwave integrated circuits (MICs) have a number of ground points all connected to a common ground plane. In the case of monolithic MICs (MMICs) this is normally the back side of the chip. When packaged it is normal to provide a low inductance ground (such as a metal based package) for the common chip ground. The inductance between the chip ground (internal to the package) and the circuit ground (external to the package) is termed the common lead ground inductance.

A fraction of the output signal is fed directly back to the input. At low frequencies, where the reactance of L_{COMMON} is small, this has minimal effect, but as the frequency of operation increases so the reactance of L_{COMMON} and hence the level of feedback increases. The presence of L_{COMMON} causes feedback between each and every pin of the package. Differential signals do not suffer from this problem, only single-ended signals.

The transceiver configuration of Figure 1 suffers from problems relating to common lead grounding inductance when low cost packaging is used. Common lead inductance serves to act as series feedback between each and every pin of the transceiver package. Just 0.2nH will act as -20dB of feedback (considering 50 ohm source and load impedances) at 2.4 GHz (the USA's ISM band). This causes the following problems:

1. Potential for instability in both transmit and receive paths as a result of loop gains greater than unity between port 5 and port 19 (the port by means of which filter 1 is connected to amplifiers 7, 17).

2. Degradation of filter performance as a result of low isolation between port 19 and port 21 (the port by means of which filter 1 is connected to mixer 9).

3. Appreciable levels of transmit power fed back to the PLL drive port 25 (can cause a radio to loose lock).

One possible solution to these problems is to provide each ground connection point on the chip with an individual package pin for connection to the external ground. With circuits containing high levels of functionality, as the transceiver of Figure 1, this results in a requirement for a package with a prohibatively large number of pins. Both cost and size of the end component are increased.

According to the present invention there is provided an integrated transceiver circuit packaged component including a transceiver circuit having a filter provided therein for filtering both the received and transmitted signals to remove unwanted components therefrom.

Preferably, the filter is a bandstop filter.

An integrated transceiver circuit packaged component in accordance with the present invention will now be described, by way of example, with reference to the accompanying drawings, in which:

Figure 1 is a circuit diagram of a prior art such component together with external filter;

Figure 2 illustrates the problem of common lead grounding inductance which occurs with the transceiver of Figure 1;

Figure 3 is a circuit diagram of the component according to the present invention together with an external filter; and

Figure 4 shows the circuit of a bandstop filter of the component of Figure 3.

In the transceiver circuit of Figure 3 the same components as those of the circuit of Figure 1 are labelled with the same reference numerals.

With a view to overcoming problems 1 to 3 above the circuit of Figure 1 has been modified. A differential drive is used for the PLL. This will

eliminate any RF signals which would be fed back in common mode. Thus, amplifier 23 of Figure 1 has been replaced by differential amplifier 27 of Figure 3. Filter 1 has been moved to the T/R common port 5 of the chip and an on-chip, bandstop filter 29 with more modest rejection of the image/unwanted sideband signals has been added between the amplifiers 7, 17 and mixer 9. Greater than 1OdB is sufficient to give significant imunity to image noise on receive and to avoid saturation of the power amplifier 17 on transmit. A suitable compact circuit for the bandstop filter 29 comprising a combination of series and shunt bandstop L, C elements is shown in Figure 4. Filter 29 rejects the image/unwanted sideband (at frequency LO -IF) but does nothing to reject harmonics/spurious responses at other frequencies. The band pass filter 1 at the T/R common port 5 serves this purpose. Further, any external ground returns from the circuitry at the control port of the VCO 3 should be eliminated.

The transceiver architecture of Figure 3 is much more tolerant to common lead ground inductance. The only single-ended signals coming from the chip are from the T/R common port 5, that is not more than one single-ended signal is input to/output by the chip in either mode of operation. Because all other inputs/outputs are differential or DC/control, the chip is very tolerant to portions of the single-ended signal at the common port 5 being fed back to other ports as a result of the common lead ground inductance. Thus, low cost plastic packaging can be used.

If a transceiver chip were fabricated which used an off-chip local oscillator drive, the differential drive the PLL would not be required nor would the elimination of the external ground returns from the local oscillator control circuitry, although the local oscillator drive would need to be either differential or at a very low signal level to avoid saturation of the low noise amplifier 7 in receive mode.

If an on-chip resonator and varactor were used then the aforementioned elimination of external ground returns would be observed by default. If an on-chip balanced VCO were used, ground connections could be made at virtual earth points without causing RF current to flow in the common lead inductance.

Claims

1. An integrated transceiver circuit packaged component including a transceiver circuit having a filter (29) provided therein for filtering both the received and transmitted signals to remove unwanted components therefrom.

2. A component according to Claim 1, wherein said filter (29) is a bandstop filter (29).

3. A component according to Claim 2, wherein said transceiver circuit includes a mixer (9) for mixing a locally generated frequency with the received signals when the transceiver circuit is being used in receive mode and with the transmitted signals when the transceiver circuit is heing used in transmit mode, said filter (29) being connected between said mixer (9) and a common input/output port (5) of said circuit.

4. A component according to Claim 3, wherein said transceiver circuit includes a voltage controlled oscillator (3) for providing to said mixer (9) said locally generated frequency.

5. A component according to Claim 4, wherein said transceiver circuit has a phase locked loop (PLL) drive output and includes connected thereto a PLL differential amplifier (27) for providing a signal at the PLL drive output by amplifying a signal derived from the output of the voltage controlled oscillator (3).

6. A component according to Claim 3 or Claim 4 or Claim 5, wherein said transceiver circuit includes between said filter (29) and said input/output port (5) a low noise amplifier (7) for amplifying the received signals, a power amplifier (17) for amplifying the transmitted signals, and switch means for connecting either the low noise amplifier (7) or the power amplifier (17) between the filter (29) and the input/output port (5).

7. A component according to Claim 6, wherein said transceiver circuit includes between an intermediate frequency output (13) thereof and said mixer (9) a first differential amplifier (11), and between an intermediate frequency input (15) thereof and said mixer (9) a second differential amplifier (12), said transceiver circuit further including further switch means between the first and second differential amplifiers (11,12) and said mixer (9) by means of which the mixer (9) may be connected to either the first (11) or second (12) differential amplifier, said first and second differential amplifiers (11,12) being operable to amplify the received and transmitted signals respectively.

8. A component according to any one of Claims 3 to 7 in combination with a bandpass filter (1) connected to said input/output port (5) for filtering both the received and transmitted signals.

Fig.1.

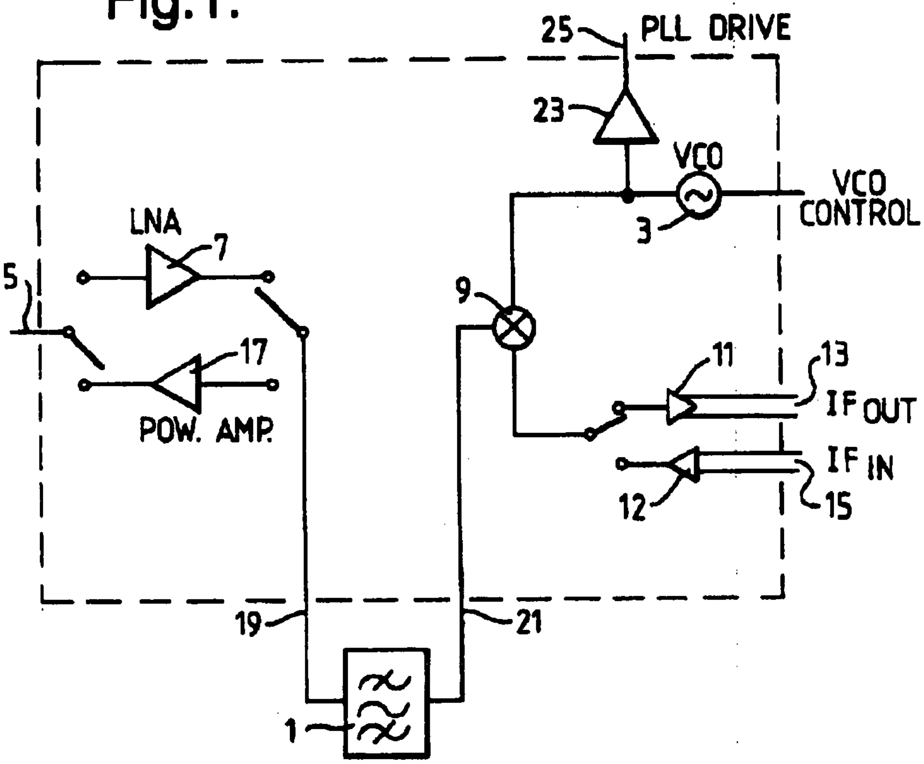

25
PLL DRIVE
23
VCO
VCO
CONTROL
3
LNA
7
5
9
17
11
13
IF OUT
POW. AMP.
IF IN
12
15
19
21
1

Fig.2.

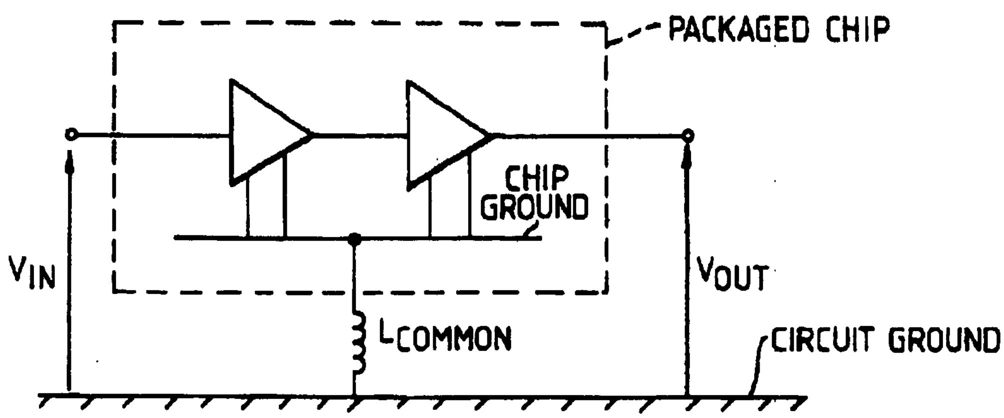

PACKAGED CHIP
CHIP
GROUND
V IN
V OUT
L COMMON
CIRCUIT GROUND

Fig.3.

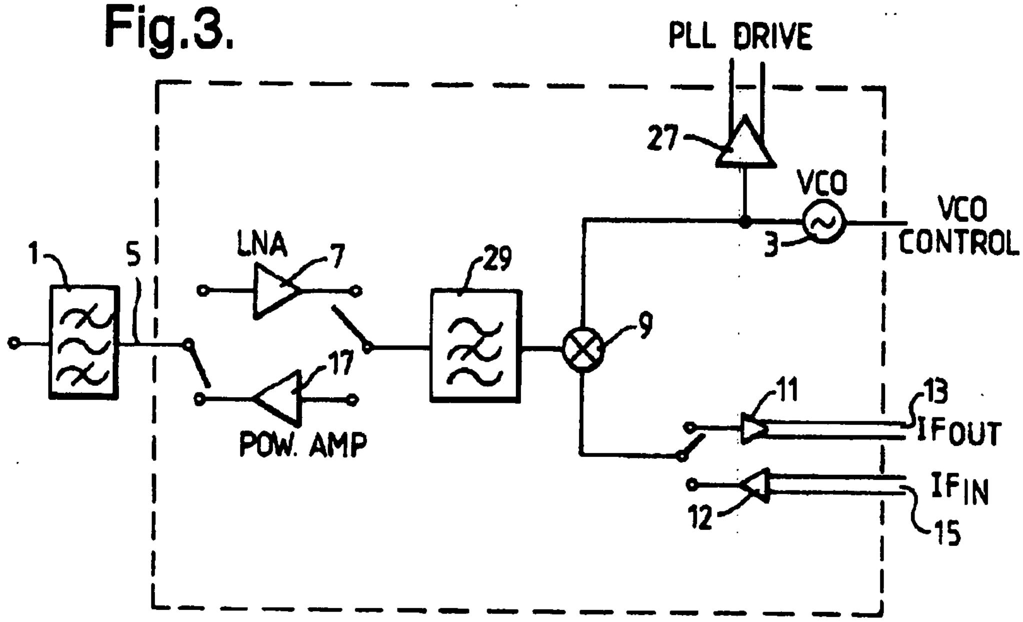
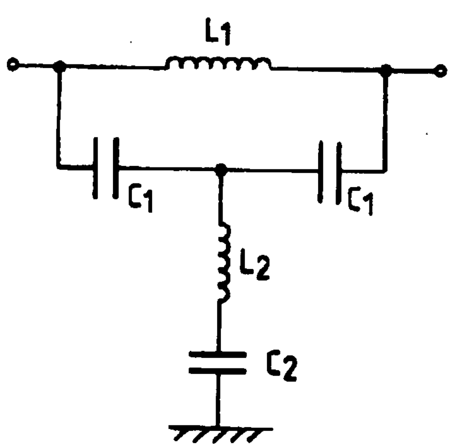

PLL DRIVE
27
VCO
VCO CONTROL
3
1
5
LNA
7
29
9
17
POW. AMP
11
13
IFOUT
IFIN
12
15

Fig.4.


L1
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EUROPEAN SEARCH REPORT

Application Number
EP 94 30 2424

DOCUMENTS CONSIDERED TO BE RELEVANT

Category	Citation of document with indication, where appropriate, of relevant passages	Relevant to claim	CLASSIFICATION OF THE APPLICATION (Int.Cl.5)
A	PROCEEDINGS OF THE NINETEENTH INTERNATIONAL SYMPOSIUM ON GALLIUM ARSENIDE AND RELATED COMPOUNDS, Karuizawa, Japan, 28 September-2 October 1992. Kermarrec et al. : "High performance, low cost GaAs MMICS for personal phone applications at 1.9GHz" * figure 1 *	1	H04B1/40
A	WO-A-85 00481 (MOTOROLA, INC) * abstract; figures 1,3 *	1,3,4,6, 8	
A	US-A-4 792 939 (HIKITA ET AL.) * claim 1; figure 1 *	1	
A	US-A-5 202 651 (YOSHIMASU) * column 3, line 19 - column 68; figure 5 *	2,3	
			TECHNICAL FIELDS SEARCHED (Int.Cl.5)
			H04B

The present search report has been drawn up for all claims

Place of search	Date of completion of the search	Examiner
THE HAGUE	29 June 1994	Goulding, C

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